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ERF1002, Extreme Low Power Bluetooth 5.0 SoC Module

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Document Information

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Product status

(MP) Mass Production

This document applies to the following products:

Name	Type number	version	Product status
ERF1002	**ERF1002**	**1.0**	MP (Mass Production)

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ERF1002, Extreme Low Power Bluetooth 5.0 SoC Module

Contents

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1 Functional description

1.1 Product overview

The ERF1002 module is an extreme low-power Bluetooth® 5 system-on-a-chip (SoC) solution. This innovative module design is based on the extremely low power Atmosic M2 Series Bluetooth wireless platform. The ERF1002 design incorporates several innovative features that have a dramatic impact on extending the battery life of edge-of-network connected IoT products. This Bluetooth SIG certified Bluetooth Low Energy SoC integrates a Bluetooth 5.0 compliant radio with an ARM® Cortex® M0 application processor, 128 KB, 512 KB or 1MB embedded Flash, 128 KB Random Access Memory (RAM), 256 KB Read-Only Memory (ROM), 4 KB One-Time-Programmable (OTP) memory, and state-of-the-art power management.

The extremely low power ATM2 series SoC with 900uA active Rx and 2.4 mA active Tx full system power and has been designed to extend battery life for the Internet-of-Things (IoT) applications. Support for low duty cycle operation allows systems to run for significantly longer time periods without battery replacement.

1.2 Product features

- Compliant with Bluetooth 5.0 standard
- Supports Bluetooth 2 Mbps, 1 Mbps, 500 kbps, and 125 kbps (Coded Phy supports the latest long-distance and high-speed capabilities)
- Fully integrated RF front-end
- Incorporates a second specialized Wake Up Receiver (WURx) can run with the system in hibernate mode using less than 850nA in place of beaconing
- Smart sensor hub with out of bounds exception handling that can run in hibernate mode in conjunction with the Wake-Up Receiver
- SoC typical power consumption with 3 V battery including PMU
  - Active Rx @ -95 dBm: 900 uA
  - Active Tx @ 0 dBm: 2.4 mA
  - Retention @ 32 KB RAM: 2 μA
  - Hibernation with Wakeup Receiver: 0.95 μA
  - Hibernate: 0.8 μA
  - Soc Off: 300 nA
- CPU: 16 MHz ARM Cortex M0 processor, programmable interrupt router
- Memory: 128 KB, 512 KB or 1 MB embedded Flash, 256 KB ROM, 128 KB RAM, and 4 KB OTP
- Retention RAM configuration: 16 KB to 128 KB in 16 KB step sizes
- Interfaces: I2C, SPI, UART, GPIO
- 10-bit application ADC (*Note #1*)
- Digital microphone Input (PDM) (*Note #1*)
- 32.768 kHz/16 MHz crystal oscillator
- SWD for interactive debugging
- AES 128 hardware
- True random number generator (TRNG)
- Smart Sensor Hub (*Note #1*)
- Keyboard matrix controller (KSM) (*Note #1*)
- Quadrature decoder for mouse input (QDEC) (*Note #1*)
- 32.768 kHz/16 MHz crystal oscillator
- 1.1 V to 3.3 V battery input voltage with integrated Power Management Unit (PMU)

Note#1: This module is made to perform the very best of Bluetooth 5.0 functions with extremely low power. Although there are diversities of other features in the SoC which are remained in this module but are beyond the scope of this datasheet.

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2 General Specifications

Radio Transceiver
- Typical -94dbm RX sensitivity(255-byte packets,1 Mbps LE)
- TX output power from -20 dBm to +4 dBm

True single-chip BLE Soc Solution
- Integrated BLE radio
- Supports OTA programming mechanism for firmware upgrade
- Complete BLE protocol stack and application profiles
- Supports both master and slave modes
- Supports 2 Mbps LE
- Frequency bands: 2402 MHz to 2480 MHz
- GFSK modulation format
- Standard firmware AT-command stack (*Note #1*)

Very low power consumption
- Single 1.1V to 3.3V power supply
- Integrated DC-DC and LDO
- 0.85 uA power-down mode(Wakeup by Receiver)
- 2.0 uA deep sleep mode (32KHz RO on,160k SRAM in retention state)
- 900 uA Rx and 2.4 mA Tx current @0 dBm Tx power with DC-DC
- 4.0 mA Tx current @4 dBm Tx power with DC-DC

Module Size
- 14.0 X 8.5 X 2.0 mm ±0.3 mm PCB SMD

High-level integration
- 6 channel, 10 bit ADC
- 32 KHz sleep timer
- programmable PWM
- 1 channel SPI interface
- 1 channel UART interface
- 1 channel I2C master interface
- AES128 security coprocessor

Memory
- Internal 1MB embedded Flash

Part number	Embedded Flash Memory size
ERF1002	1MB

Note#1: Other firmware images/examples can be loaded onto the module to customize the functionality.

This is the customers own responsibility and support can't be delivered for custom firmware images.
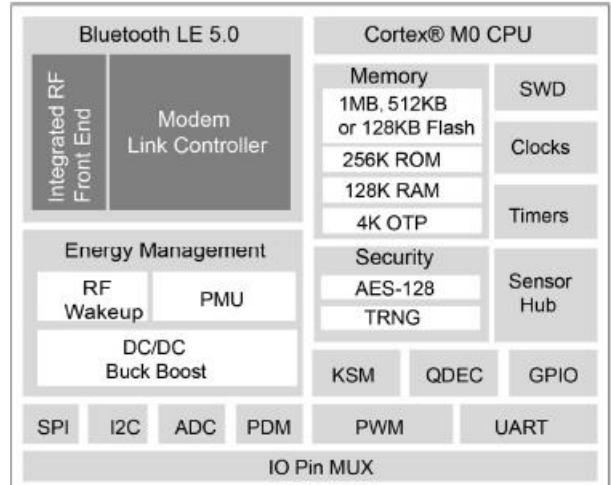
Typical applications

Industrial and Enterprise
- Beacons
- Remote Sensors
- Environmental Monitors

Healthcare
- Asset Trackers
- Locating
- Wearables

Home
- Home Automation
- Remote Control
- Human Interface Devices (HID)
- Entertainment

Smart Cities
- Asset Trackers
- Beacons

Personal
- Gaming
- Wearables

Cars
- Key fobs and Accessories
- Infotainment

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3 Electrical Specifications

3.1 Recommended Operating conditions

Operating Condition	Description	Min.	Typ.	Max.	Unit
Operating temperature range	OP-temping temperature range	-40	25	85	˚C
Relative Humidity	Humidity	-	-	85	%
VDDIO	I/O supply	1.7	1.8	3.3	V
VBAT	Battery supply	1.1		3.3	V
VPP25	OTP Programming Voltage	2.3	2.5	2.7	V
VIO	I/O pin voltage	-0.2		VIO + 0.2	V
32K-OSC	Crystal OSC-32.768 kHZ	-500		500	ppm

Notes:

1. VBAT minimum supply after boot is 1.0V
2. VBAT minimum slew rate is 0.3V/ms
3. VPP25 is physically connected to VDDIO. Set VDDIO within VPP25 range when programming the OTP.

3.2 Maximum Electrical Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
VBAT	Battery supply	-0.2		3.4	V
VDDIO	I/O supply	-0.2		3.4	V
VIO	I/O pin	-0.2		3.4	V
VRF	RF I/O pin (BT_RF, WURX)			10	V
ESD (HBM)	ESD HBM class 2			2000	V
ESD (CDM)	ESD CDM			500	V
T-store	Storage Temperature	-40		125	˚C

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3.3 Radio Transceiver characteristics (VCC = 3.0V Temperature = 27˚C)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Frequency range		2.402		2.480	GHz
Rx sensitivity	**37-byte packets, clean Tx**				dBm
	- 125 kbps	-101			
	- 500 kbps	-98.5			
	- 1 Mbps	-95			
	- 2 Mbps	-93			
	255-byte packets, dirty Tx				
	- 125 kbps	-100			
	- 500 kbps	-96.5			
	- 1 Mbps	-94			
	- 2 Mbps	-91			
Tx output power	4, 2, 0, -2, -4, -6, -8, -20	-20		4	dBm
Tx power accuracy			+ /- 1.5		dB
Tx spectral mask @ 1M sym/s	2 MHz offset	-20			dBm
	> 3 MHz offset	-30			
Rx carrier-to0-Interferer (LE 1M PHY)	Co-channel interference	21		-100	dB
	Adjacent 1 MHz interference	15			
	Adjacent 2 MHz interference	-17			
	Adjacent 3 MHz Interference	-27			

3.4 Wakeup Receiver Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Sensitivity (>= 90% wakeup success rate)	2440 MHz, 14-byte packets at 1ms interval for 40ms		-44		dBm

3.5 GPIO Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input VIL		-0.2	0	0.2	V
Output VOH	2 mA Load		VIO - 0.2		V
Output VOL	2 mA Load		0.2		V

3.6 Embedded Flash Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Endurance	Program/Erase	100.000			Cycles
Data Retention			20		Years

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3.7 Power consumption

Parameter	Conditions	Min.	Typ.	Max.	Unit
Active Rx	Sensitivity at -95 dBm 1 mA		1		mA
Active Tx @ 4 dBm	Output power at 4 dBm		4		mA
Active Tx @ 0 dBm	Output power at 0 dBm		2.5		mA
Active Tx @ -10 dBm	Output power at -10 dBm		1.4		mA
Powerdown	PWD pin asserted		75		nA
Retention (32 KB RAM)			2		µA
Hibernation			0.8		µA
Hibernation with Wakeup Receiver			0.95		µA
SoC Off			300		nA

3.8 PMU Configuration

There is a PMU (Power Management Unit) inside the SoC, below is the description of these power rails.

Power rail	Pin on module	Input / Output	Description
VBAT	6	I	Battery or external power supply (DC 1.1 to 3.3V)
VDDIO	19	I	Power input for digital and analog I/O
VDDIOP	10	O	1.8V I/O power output generated by PMU
VAUX	12	O	The auxiliary power output of typical 3.2V used internally by the PMU

The PMU must be configured correctly to ensure correct operation. The following rules must be followed.

1. Use external VDDIO power supply (One external power supply or battery with external IO supply)

- VBAT to external power or battery
- Connect VBAT to VDDIO
- Connect VAUX to VDDIOP
- Disable IO supply generation (*Note #2*)

2. Use the internal VDDIO power supply (One external power supply or battery with internally generated IO supply)
This is for the application that can use an internal 1.8V IO supply for better power consumption or
VBAT<=1.8V

- VBAT to external power or battery
- Connect VDDIOP to VDDIO

Note #2: Internal I/O supply VDDIOP can be disabled in firmware by controlling the register opt_disable_vddio, and it will not be discussed here. The internal I/O supply is enabled by default.

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3.9 BT5.0 BLE RF Performance test

Sample under test: ERF1002
Test machine: IQ2011
Data rate: 1Mbps

Item / channel / Packet type	No.		Tx power (-20 to 20dBm)			Frequency offset (-150 to 150MHz)			Sensitivity (≤ 70dBm)		
			2402MHz	2442MHz	2480MHz	2402MHz	2442MHz	2480MHz	2402MHz	2442MHz	2480MHz
Ble_1M_prbs9	1#		2.29	2.15	1.73	-60	-61	-60	-96.0	-96.0	-97.0
Ble_1M_prbs9	2#		3.4	3.16	2.84	-62	-61	-60	-96.5	-96.5	-97.0
Ble_1M_prbs9	3#		3.68	3.62	3.35	-61	-61	-62	-95.0	-96.0	-96.0
Ble_1M_prbs9	4#		4.01	3.77	3.54	-60	-62	-62	-94.0	-95.0	-95.0
Ble_1M_prbs9	5#		4.03	3.78	3.53	-61	-62	-59	-95.0	-95.0	-95.0

1. Test sensitivity:
   - Sent 100~1500 packets@PER≤30.8%
   - packets type: BT_LE PRBS9
   - packets length: 37 bytes

2. Max input level ≥-10dBm.

Result: OK

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4 Mechanical specifications

4.1 Pin Assignment

Pin	Pin Name	I/O	Description	GPIO
1	GND	PWR	Ground	
2	BT_RF	RF	2.4GHz Single-ended RF I/O for Bluetooth radio	
3	WURX	RF	Wake receiver RF input, connect to ext. antenna	
4	PWD	I/O	Power Down Input (Active High)	
5	GND	PWR	Ground	
6	VBAT	PWR Input	Battery Power Supply (DC 1.1 to 3.3V)	
7	UART0_CTS	I/O	UART 0 CTS	P11
8	SPI_CS	I/O	SPI Chip Select	P10
9	I2C0_SCL	I/O	I2C 0 SCL	P9
10	VDDIOP	PWR Output	1.8V I/O power supply generated by SoC, connect to VAUX if unused (see 3.8 PMU configuration)	
11	GND	PWR	Ground	
12	VAUX	PWR	Reserved for switching regulator internal use	
13	32K_OUT	A	32.768 kHz crystal oscillator output	
14	32K_IN	A	32.768 kHz crystal oscillator input	
15	SPI_MISO	I/O	SPI MISO	P13
16	SPI_CLK	I/O	SPI Clock	P20
17	SPI_MOSI	I/O	SPI MOSI	P22
18	GND	PWR	Ground	
19	VDDIO	PWR Input	Power supply input for digital I/O (see 3.8 PMU configuration)	
20	UART0_RTS	I/O	UART 0 RTS	P24
21	UART0_TX	I/O	UART 0 TX	P23
22	UART0_RX	I/O	UART 0 RX	P25
23	I2C0_SDA	I/O	I2C 0 SDA	P30
24	P32	I/O	UART 1 RX or GPIO32	P32
25	UART1_TX	I/O	UART 1 TX	P33
26	SWD_CLK	I/O	SWD_CLK – Serial Wire Debugger	P1
27	SWD_IO	I/O	SWD_IO – Serial Wire Debugger	P2
28	GND	PWR	Ground	

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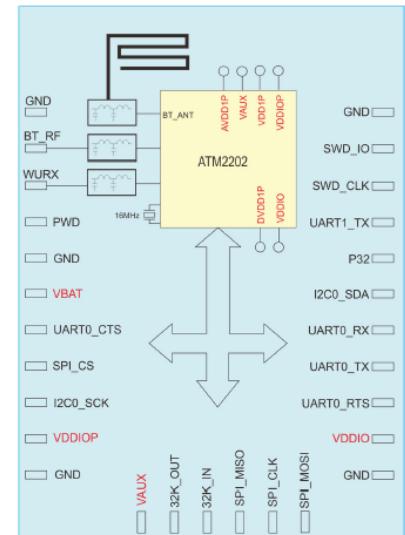
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4.2 PCB Layout

Unit: mm

RF signal is connected to the   on
board PCB trace antenna through C4
(see section-19)

The 2nd route of RF
signal is connected to
pin2 through R1
(see section-19)
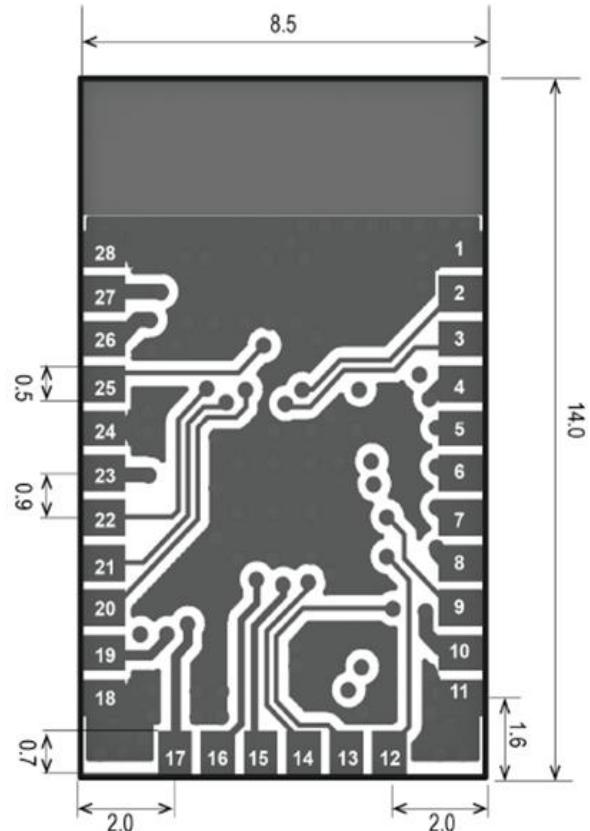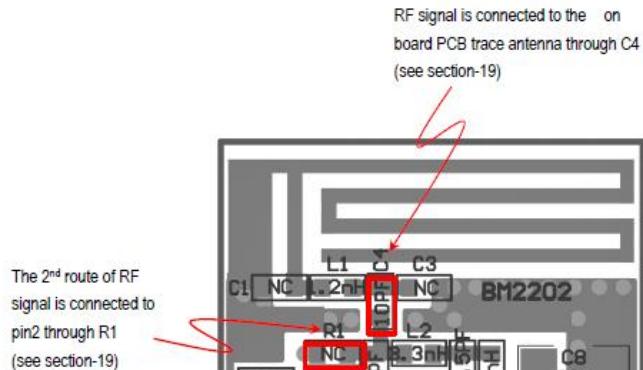
Notes:

1. Some power rails have to be externally connected, (see 3.1 Recommended Operating conditions)

2. The BT RF signal has two routes to the antenna. The 1st route goes to the PCB trace antenna through L1, The 2nd route goes to pin-2 on the module through the R1 resistor then to the external antenna, the R1 resistor is not populated as default.
   Using the external antenna gives better performance and a longer RF signal range.
   Please put on a 0-ohm resistor or 10pF capacitor at the R1 location and remove C4 (see, PCB placement top view). One SMA antenna socket is recommended in designing the carrier or host board for this antenna.

3. The WURX signal on pin-3 is input for Wake up Receiver.
   The use of a wake-up receiver allows a system to be in sleep mode while waiting for incoming RF activities. In the SoC, the wake-up receiver is designed to decode an incoming RF paging or wake-up signal with very low power consumption. This dedicated low-power wake-up receiver continuously monitors the incoming RF signal for a predefined paging signal. This continuous Rx mode is based on an OOK radio, which has ultralow power consumption. The wake-up receiver is intended for short-range and short-latency applications. The latency of the wake-up receiver is typically in the order of 20 ms to 1 s, depending on the length of the Rx ID code used to identify the target device.
   In designing the carrier or host board, an SMA antenna socket is recommended going through a serial 10pF capacitor.

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5 Recommended Reflow Profile

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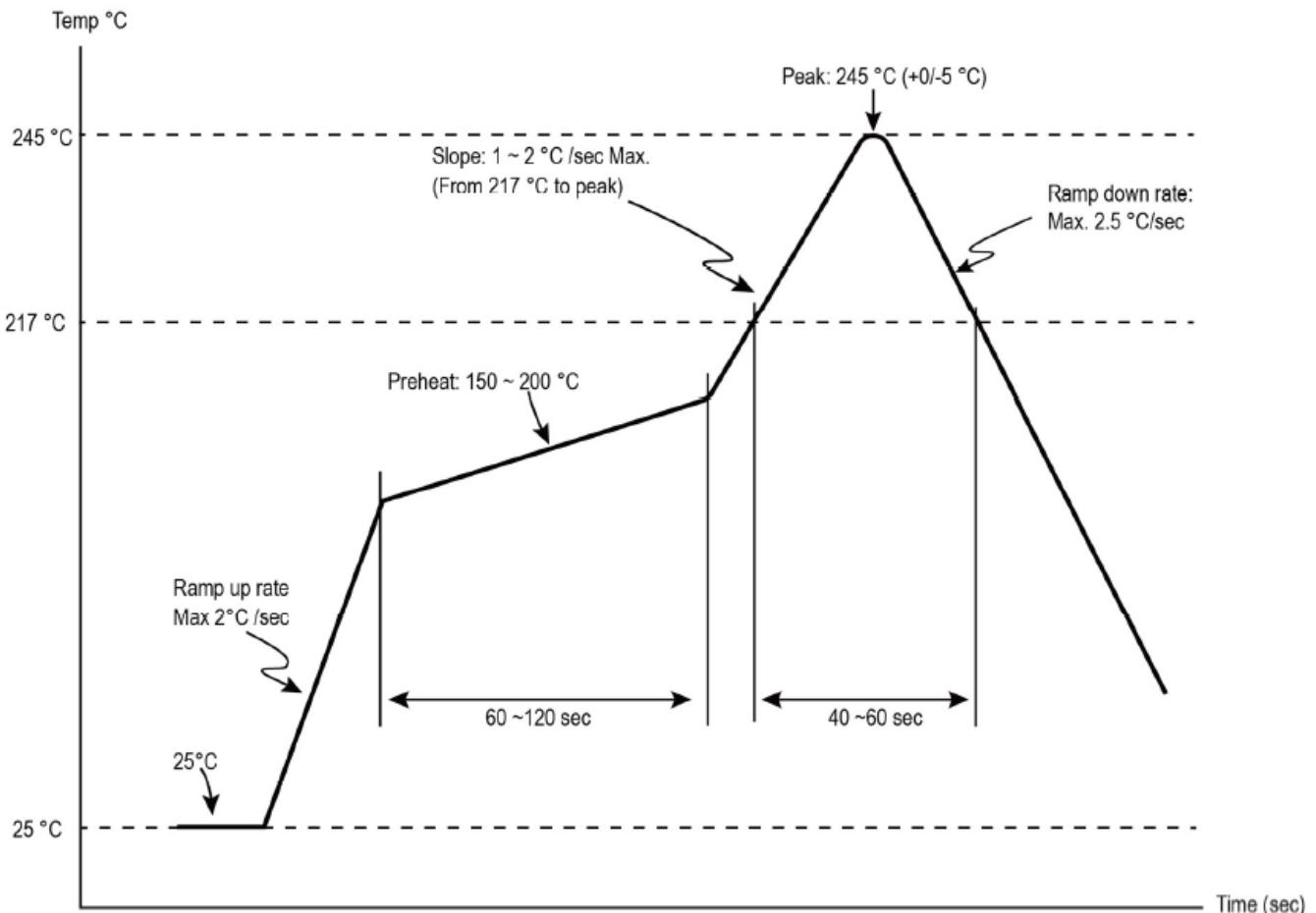
6 Evaluation Board (EVB)

Below you can find an image of the ERF1002 EVB board.

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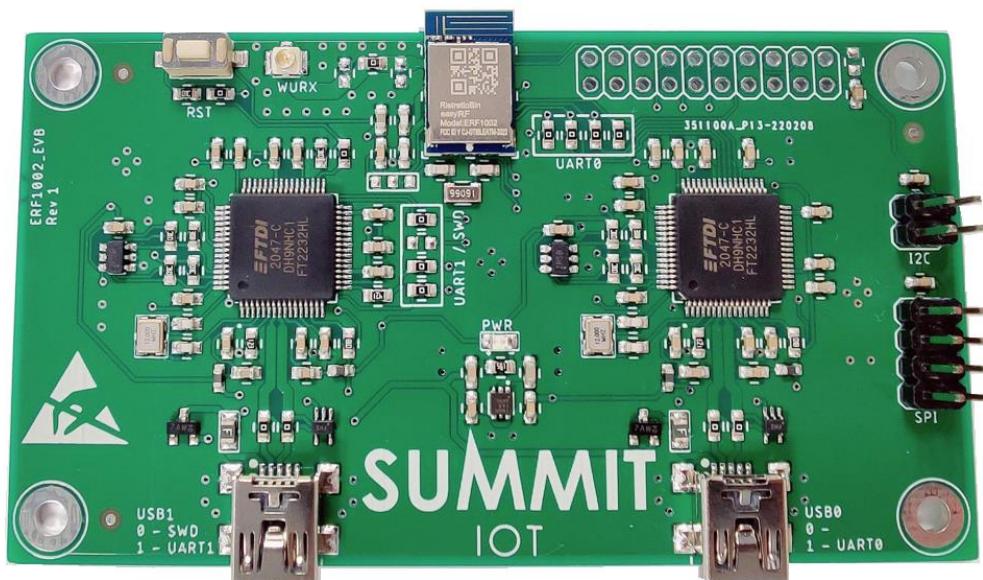
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7 Packaging

28±1

330±2

After vacuum
loading into
the inner box

inner box

Loading 1700pcs product,
(20 spaces before and
after, without products.)

inner box K3K:
33.5cm*34.7cm*7cm

1、Loading 1700pcs product into carrier tape
  (20 spaces before and after, without products)
2、After the tape is finished, vacuum packaging
is carried out。
3、After vacuum loading into the inner box.
(1700pcs/BOX)
4、1700pcs*5=8500pcs / Outer box

5 inner boxes

Outer box K=A:
36.4*35.7*37.5cm

The ERF1002 is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although ERF1002 is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.

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ITEM	W	A0	B0	K1	K0	P	F	E	D0	D1	P0	P2	T
DIM	24.0 +0.30/-0.30	9.90 +0.10/-0.10	14.60 +0.10/-0.10	---	+0.10/-0.10 2.20 +0.10/-0.10	16.0	+0.10/-0.10 14.20 +0.10/-0.10	1.75 +0.10/-0.10	ø1.5 +0.10/-0.00	ø1.5 +0.10/-0.00	4.0 +0.10/-0.10	2.0 +0.10/-0.10	0.35 +0.05/-0.05

Module orientation

Direction of unreeling
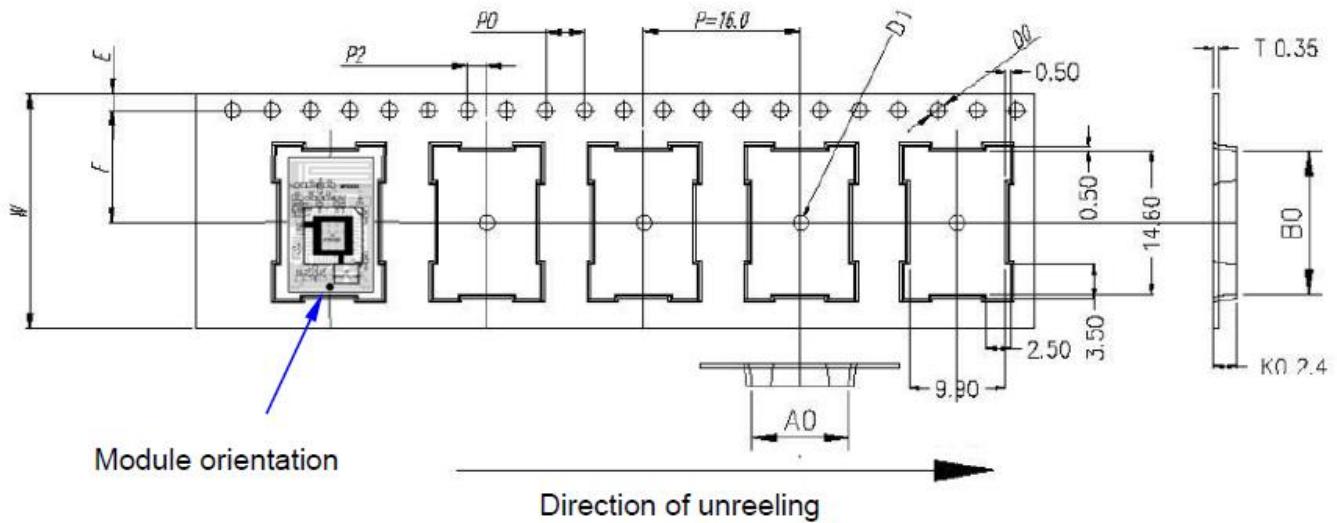
Ordering information

Ordering can be done via www.summit-electronics.com or via info@summit-electronics.com. Please contact us for more information. Customisation of the product is available on request.

Technical support

For all product questions please contact us via info@summit-electronics.com

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